



ED/CPMT Chapters of IEEE Orlando Section AVS Student Chapters of UCF

Present guest lecture by

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High-k Gate Dielectrics and Metal Electrodes for Future Generation CMOS: Challenges and Opportunities

Abstract: Although the ITRS suggests that low power applications may require high-k materials first, the high performance device trend will soon require both high-k dielectrics and metal gate electrodes to remove poly depletion effects. Realization of high performance devices with high-k/metal gates has been limited primarily due to commonly observed mobility degradation and restricted threshold voltage control. Recent developments indicate that devices with carrier mobility comparable to state of art oxynitride gate dielectrics can be achieved, however, identification and integration of suitable metal gates still remains a major challenge. To achieve suitable Vt for n and pMOSFETs it is essential to utilize metal gates with appropriate near band-edge work function. This presentation will discuss the challenges and opportunities in identifying candidate material systems and associated processing techniques for future generation CMOS gates. Additionally, the influence of these gate materials and processing on the underlying dielectric stack due both to its chemical reactivity and nature of processing will be addressed.

Bio: Prashant Majhi received the Ph.D. degree in science and engineering of materials program from Arizona State University, Tempe, AZ (2000), and the Bachelors of Technology degree from the Indian Institute of Technology, Madras (1996). He joined the process development group at Philips Semiconductors in the Netherlands in 2000 and had been the project leader in module development for several CMOS and mixed signal process technologies. In Oct 2004, he joined Intel Corp., and is at SEMATECH as an Intel Assignee managing the Advanced Gate Electrodes group. He has authored or co authored more than 75 papers in journals and conferences and holds several IC process development patents.

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